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CLAIM AMENDMENTS:

Claim 1 (Previously Presented): A rearrangement sheet adapted to be mounted on a top surface of an element, comprising:

an insulating sheet having a smaller size in area than the top surface of the element, said insulating sheet having an element mounting region defined thereon; and

a plurality of conductive metallic patterns formed on the insulating sheet so as to surround, and not extend into, the element mounting region, each of said conductive metallic patterns extending continuously, and in a straight line.

Claim 2 (Original): The rearrangement sheet according to claim 1, wherein said conductive metallic patterns comprise electrodes for wire bonding with external electrodes.

Claim 3 (Original): The rearrangement sheet according to claim 1, wherein said conductive metallic patterns are metallic wiring patterns.

Claim 4 (Original): The rearrangement sheet according to claim 1, wherein said conductive metallic patterns are conductive metal plated patterns.

Claim 5 (Previously Presented): The rearrangement sheet according to claim 4, wherein said conductive metallic patterns comprise a laminated pattern of an underlying plated pattern formed on an upper surface of the insulating sheet and a conductive metal plated pattern formed on this underlying plated pattern.

Claim 6 (Previously Presented): The rearrangement sheet according to claim 1, wherein an insulating adhesive sheet is provided in the element mounting region.

Claim 7 (Original): The rearrangement sheet according to claim 1, wherein said insulating sheet is an insulating adhesive sheet.

Claim 8 (Currently Amended): A semiconductor device comprising:

a substrate;

a first element provided with a plurality of first bonding pads, and being disposed in a first element formation region on an upper surface of the substrate;

a second element provided with a plurality of second bonding pads, the second element being disposed over an upper side of the first element;

a plurality of bonding posts provided on the upper surface of said substrate, and outside so as to surround the first element formation region;

first wires that electrically connect respective ones of the bonding posts with respective ones of said first bonding pads; and

a rearrangement sheet provided with an insulating sheet, and a plurality of conductive metallic patterns that are formed on the insulating sheet, the rearrangement sheet being provided between said first element and said second element;

wherein said conductive metallic patterns are formed in a region exposed from said second element, so that the conductive metallic patterns surround, and do not extend under, the second element, said conductive metallic patterns each including a first portion that can be reached by a straight line extending from another respective

one of the bonding posts for a second pad connection, without contacting or crossing said first bonding pads, and a second portion, capable of wire bonding with a respective one of the second bonding pads, thereby coupling the another respective one of the bonding post to the second bonding pad;

the first portions and the ~~respective~~ another respective ones of the bonding posts being electrically connected by first relay wires; and

said second portion and said respective ones of the second bonding pads being electrically connected by second relay wires.

Claim 9 (Previously Presented): The semiconductor device according to claim 8, wherein said conductive metallic patterns include an underlying plated pattern formed on an upper surface of said insulating sheet, and a conductive metal plated pattern formed on the underlying plated pattern.

Claim 10 (Previously Presented): The semiconductor device according to claim 8, wherein said conductive metallic patterns are metallic wiring patterns formed on an upper surface of said insulating sheet.

Claim 11 (Previously Presented): The semiconductor device according to claim 8, wherein said conductive metallic patterns comprise a metallic wiring pattern formed on an upper surface of said insulating sheet and conductive metal plated patterns provided on the metallic wiring patterns including the first portion and including the second portion.

Claim 12 (Previously Presented): A semiconductor device, comprising:

a semiconductor element having a plurality of bonding pads formed on an upper surface thereof;

a rearrangement sheet comprising an insulating sheet and conductive metallic patterns electrically connected with said bonding pads, stuck onto the upper surface of the semiconductor element other than in a region where the bonding pads are formed so as to be surrounded by the bonding pads; and

a sealed portion that seals the upper surface of said semiconductor element so as to cover said rearrangement sheet;

wherein said conductive metallic patterns comprise rearrangement posts of a same number as said bonding pads, wire connection portions of the same number as the bonding pads, the rearrangement posts and the wire connection portions being arranged so that the rearrangement posts are surrounded by the wire connection portions, and rewiring leads that connect said rearrangement posts and said wire connection portions;

said wire connection portions and said bonding pads are connected by metallic wires,

conductive posts are formed on an upper surface of said rearrangement posts; and

part of the conductive posts is exposed from said sealed portion.

Claim 13 (Original): The semiconductor device according to claim 12, wherein said conductive metallic patterns are conductive metallic wiring patterns.

Claim 14 (Original): The semiconductor device according to claim 12, wherein said conductive metallic patterns are conductive metal plated patterns.

Claim 15 (Previously Presented): The semiconductor device according to claim 12, wherein, of said conductive metallic patterns, said rearrangement posts and said rewiring leads are constituted by first metallic wiring patterns; and

said wire connection portions are constituted by second metallic wiring patterns and conductive metal plated patterns formed on the second metallic wiring patterns.

Claim 16-20 (Cancelled).

Claim 21 (Previously Presented): The rearrangement sheet according to claim 1, wherein said conductive metallic patterns are disposed directly on a surface of said insulating sheet.

Claim 22 (Previously Presented): The rearrangement sheet according to claim 1, wherein each of said conductive metallic patterns extends levelly from an edge of said insulating sheet to the element mounting region.

Claim 23 (Previously Presented): The rearrangement sheet according to claim 1, wherein the conductive metallic patterns are disposed at a north, south, east and west side of the element mounting region.

Claim 24 (Previously Presented): The rearrangement sheet according to claim 1, wherein the element mounting region is adapted for mounting a semiconductor element therein.

Claim 25 (Previously Presented): In combination, an element having a top surface; and a rearrangement sheet mountable on the top surface of the element, the rearrangement sheet including:

an insulating sheet having a smaller size in area than the top surface of the element, the insulating sheet having an element mounting region defined thereon; and

a plurality of conductive metallic patterns formed on the insulating sheet so as to surround, and not extend into, the element mounting region, each of the conductive metallic patterns extending continuously, and in a straight line.

Claim 26 (Previously Presented): The combination according to claim 25, wherein the conductive metallic patterns comprise electrodes for wire bonding with external electrodes.

Claim 27 (Previously Presented): The combination according to claim 25, wherein the conductive metallic patterns are metallic wiring patterns.

Claim 28 (Previously Presented): The combination according to claim 25, wherein the conductive metallic patterns are conductive metal plated patterns.

Claim 29 (Previously Presented): The combination according to claim 28, wherein the conductive metallic patterns comprise a laminated pattern of an underlying plated pattern formed on an upper surface of the insulating sheet and a conductive metal plated pattern formed on this underlying plated pattern.

Claim 30 (Previously Presented): The combination according to claim 25, further comprising an insulating adhesive sheet provided in the element mounting region.

Claim 31 (Previously Presented): The combination according to claim 25, wherein the insulating sheet is an insulating adhesive sheet.

Claim 32 (Previously Presented): The combination according to claim 25, wherein the conductive metallic patterns are disposed directly on a surface of the insulating sheet.

Claim 33 (Previously Presented): The combination according to claim 25, wherein each of the conductive metallic patterns extends levelly from an edge of the insulating sheet to the element mounting region.

Claim 34 (Original): The combination according to claim 25, wherein the conductive metallic patterns are disposed at a north, south, east and west side of the element mounting region.

Claim 35 (Previously Presented): The combination according to claim 25, further comprising a semiconductor element mountable in the element mounting region.